

## CLAIM LISTING

11. (previously presented): A method comprising:

querying whether a set of data resides in a cache memory that is  
communicatively coupled to a processor unit;

receiving an indication at the processor unit from the querying which  
indicates whether the set of data resides in the cache memory; and

communicating the indication to an operating system being executed on the  
processor unit.

12. (cancelled).

13.(original): A method as described in claim 11, further comprising  
establishing a relative amount of time to access the set of data by the  
processor unit based on the indication which indicates whether the set of  
data resides in the cache memory.

14.(original): A method as described in claim 11, wherein the set of data is  
selected from the group consisting of:  
an instruction for controlling the processor unit; and  
data for being processed by the processor unit.

15.(original): A method as described in claim 11, wherein the cache memory is

1       selected from the group consisting of:

2       a cache memory for storing an instruction for controlling the processor unit;

3       a cache memory for storing data for being processed by the processor unit;

4       and

5       a combination of the forgoing.

6  
7       16.(original): A method as described in claim 11, wherein the querying and the  
8       receiving are performed without reading the set of data from the cache  
9       memory to the processor unit and without writing the set of data from the  
10       processor unit to the cache memory.  
11

12  
13       17.(original): A method as described in claim 11, further comprising:  
14       comparing an address of the set data with at least one other address in the  
15       cache memory, wherein the cache memory includes a plurality of levels; and  
16       providing, based on the comparing, an indication to the processor unit of  
17       whether the address of the set of data is included in the cache memory, wherein if  
18       the address is included in the cache memory, the indication indicates at which  
19       level of the plurality of levels the address is included.  
20

21  
22       18.(original): One or more computer-readable media comprising computer-  
23       executable instructions that, when executed, perform the method as recited  
24       in claim 11.  
25

19. (previously presented): A method comprising:

comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;

providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;

establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and

communicating the indication, by the processor unit, to software being executed on the processor unit.

20. (cancelled).

21. (original): A method as described in claim 19, wherein the software is selected from the group consisting of an operating system and an application.

22. (original): A method as described in claim 19, wherein the cache memory is selected from the group consisting of:

1 a cache memory for storing an instruction for controlling the processor unit;  
2 a cache memory for storing data for being processed by the processor unit;  
3 and  
4 a combination of the forgoing.

5  
6 23.(original): One or more computer-readable media comprising computer-  
7 executable instructions that, when executed, perform the method as recited  
8 in claim 19.

9  
10 Claims 23-13 (cancelled).

11  
12  
13 42.(previously presented): For use on a processor unit that is communicatively  
14 coupled to a comparison unit that is communicatively coupled to a cache  
15 memory, a cache residency test instruction, which when executed on the  
16 processor unit, configures the comparison unit to perform acts comprising:  
17 comparing an address received from the processor unit with an address in  
18 the cache memory;  
19 providing an indication to the processor unit based on the comparing of  
20 whether the address is included in the cache memory; and  
21 communicating the indication to an operating system being executed by the  
22 processor unit.  
23  
24  
25

1 43.(original): A cache residency test instruction as described in claim 42,  
2 wherein the indication indicates to the processor unit whether the address is  
3 included in the cache memory, and if so, at which level of a plurality of  
4 levels of the cache memory the address is included.

6 44.(original): A cache residency test instruction as described in claim 42,  
7 wherein the cache memory is selected from the group consisting of:

8 a cache memory for storing an instruction for controlling the processor unit;

9 a cache memory for storing data for being processed by the processor unit;

11 and

12 a combination of the forgoing.

14 45.(previously presented): A system comprising:

15 a cache memory; and

16 a processor unit communicatively coupled to the cache memory, wherein  
17 the processor unit includes a cache residency test instruction that, when executed,  
18

19 configures the processor unit:

20 to query whether a set of data resides in the cache memory;

21 to receive an indication from the query of whether the set of data  
22 resides in the cache memory;

23 to establish a relative amount of time to access the set of data; and

24 to communicate the indication and the relative amount of time to  
25

software being executed on the processor unit.

46.(original): A system as described in claim 45, further comprising a comparison unit, wherein execution of the cache residency test instruction by the processor unit configures the comparison unit to compare an address of the set of data with at least one other address of the cache memory in response to the query.

47.(cancelled).

48.(original): A system as described in claim 45, wherein the set of data is selected from the group consisting of:  
an instruction for controlling the processor unit; and  
data for being processed by the processor unit.

49.(original): A system as described in claim 45, wherein the cache memory is selected from the group consisting of:  
a cache memory for storing an instruction for controlling the processor unit;  
a cache memory for storing data for being processed by the processor unit;  
and  
a combination of the forgoing.

1 50.(original): A system as described in claim 45, wherein the cache memory  
2 includes a plurality of levels, if the address is included in the cache  
3 memory, the indication indicates at which level of the plurality of levels the  
4 address is included.

5  
6 Claims 51-55 (cancelled).

7  
8 56.(previously presented): A processor chip comprising  
9 a processor unit having a coupling for communicatively coupling the  
10 processor unit to a cache memory, wherein:  
11

12 the processor unit includes storage for a cache residency test  
13 instruction; and

14 an execution of the cache residency test instruction with the  
15 processor unit configures the processor unit to determine if a set of data  
16 resides in the cache memory, establish a relative amount of time to access  
17 the set of data, and communicate a result of the determination and the  
18 relative amount of time to software being executed on the processor unit.  
19

20  
21 57.(original): A processor chip as described in claim 56, further comprising a  
22 second processor unit having:

23 a coupling for communicatively coupled the second processor unit to  
24 the cache memory;  
25

1 storage for a second cache residency test instruction; and

2 an execution of the second cache residency test instruction with the  
3 second processor unit configures the second processor unit to determine if a  
4 set of data resides in the cache memory and communicate a result of the  
5 determination to software being executed on the second processor unit.  
6

7 58.(original): A processor chip as described in claim 56, wherein the set of  
8 data is selected from the group consisting of:  
9 an instruction for controlling the processor unit; and  
10 data for being processed by the processor unit.  
11

12  
13 59.(original): A processor chip as described in claim 56, wherein the cache  
14 memory is selected from the group consisting of:  
15 a cache memory for storing an instruction for controlling the processor unit;  
16 a cache memory for storing data for being processed by the processor unit;  
17  
18 and  
19 a combination of the forgoing.  
20

21 60.(original): A processor chip as described in claim 56, wherein the cache  
22 memory is selected from the group consisting of:  
23 a cache memory located on the processor chip;  
24 a cache memory located off the processor chip; and  
25



a combination of the forgoing.

61.(original): A processor chip as described in claim 56, wherein the cache memory is configured as a semiconductor-based memory.

62.(original): A processor chip as described in claim 56, wherein the software is selected from the group consisting of an operating system and an application.

63.(previously presented): A computing device comprising:  
a storage device; and  
a processor chip, communicatively coupled to the storage device, and including:  
a cache memory; and  
a processor unit communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test instruction that, when executed by the processor unit, configures the processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to an operating system being executed on the processor chip.

64.(previously presented): A computing device as described in claim 63,

1 wherein the processor chip further comprises a second processor unit  
2 communicatively coupled to the cache memory, wherein the second  
3 processor unit includes storage for a second cache residency test instruction  
4 that, when executed by the second processor unit, configures the second  
5 processor unit to determine if a set of data resides in the cache memory and  
6 to communicate a result of the determination to the operating system being  
7 executed on the processor chip  
8

9  
10 65.(original): A computing device as described in claim 63, wherein the set of  
11 data is selected from the group consisting of:  
12 an instruction for controlling the processor unit; and  
13 data for being processed by the processor unit.  
14

15 66.(original): A computing device as described in claim 63, wherein the cache  
16 memory is selected from the group consisting of:

17 a cache memory for storing an instruction for controlling the processor unit;

18 a cache memory for storing data for being processed by the processor unit;

19  
20 and

21 a combination of the forgoing.  
22

23 67.(original): A computing device as described in claim 63, wherein the cache  
24 memory is configured as a semiconductor-based memory.  
25

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25

68.(cancelled).